Journal of Scientific and Innovative Research 2017; 6(3): 97-104
Available online at: www.jsirjournal.com

Research Article

ISSN 2320-4818
JSIR 2017; 6(3): 97-104

Received: 12-09-2017
Accepted: 09-10-2017

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Enhancing switching threshold for wide fan-in domino gates with shortened evaluation period

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Abstract

With technology scaling up, noise resistance has become critical in high performance VLSI chips using wide fan-in domino gates. Techniques for enhancement of noise tolerance in domino gates incur cost in terms of design metrics like power dissipation, delay and die area. Existing techniques improve noise immunity of domino gates either by precharging the internal node of PDN or controlling the evaluation period. Pre-charging the internal nodes increases switching threshold of the evaluation transistors and demands more transistors leading to overheads not desirable for wide fan-in gates. Controlling the evaluation period of clock provides protection against noise pulse duration only. In this paper, we present an approach that combines two techniques to protect the circuit against magnitude as well as width of a noise pulse in an effort to enhance the overall noise immunity of wide fan-in domino gates. Simulation results show that our technique increases noise immunity significantly. Validation of our approach in presence of PVT variations demonstrates suitability of the proposed technique for wide fan-in gates implemented in deep sub-90 nm technology.

Keywords: Domino gate, Noise immunity, ANTE, PDN, Switching threshold voltage, Transparency window.

INTRODUCTION

Domino gate is preferred in the design of high performance VLSI chips especially using wide fan-in circuits against static configuration, which is slower and occupies larger area in deep submicron technologies [1, 2]. However, switching threshold voltage of domino gates is 20% to 30% of V_{DD} against half of V_{DD} in case of the static circuits. Effects of technology scaling in current deep submicron technologies include: (i) lowered switching threshold voltage by further scale down in supply voltage [3]. (ii) increased noise at input of evaluation transistors due to increased crosstalk/interferences [4]. (iii) reduced capacitance at the dynamic node, which in turn reduces the amount of charge stored on the dynamic node. Minor charge degradation at the dynamic node may produce erroneous result. These effects of aggressive technology scaling give rise to substantial increase in deep-submicron noise, which together with other sources of disturbance e.g. process variation, can significantly degrade reliability and signal integrity of domino gates [5, 6].

Various techniques have been proposed earlier in order to mitigate the above mentioned problems. These techniques improve noise immunity of domino gates either by (i) raising switching threshold (V_T) of the evaluation transistors with the help of pre-charging the internal node [8, 10] or (ii) controlling the evaluation period [11, 12]. Raising the switching threshold voltage requires additional transistors at each input of wide fan-in configurations and causes overheads in design metrics. Apart from this, such approach is not suitable for wide fan-in circuit configuration which needs longer evaluation period and noise pulse duration can severely impact on noise immunity. Alternately, shortening the evaluation period can be effective for wide fan-in domino gates since it can be implemented with fewer transistors. However, such approach lacks protection for noise magnitude while enhancing noise immunity against the noise pulse duration/

Raising the threshold voltage of evaluation transistors along with a shortened evaluation period is obviously a desirable combination for enhancing overall noise immunity of wide fan-in domino gates. In this paper, we present a modification in Mazumdar's technique proposed earlier [12] to raise switching threshold of evaluation transistors before the evaluation period shortened to protect the circuit configuration against both magnitude and pulse width of a noise pulse and make the technique more

suitable for wide fan-in circuit configuration. We evaluate the noise immunity of our technique with reference to impact on different design metrics like power, delay and area. We also compare noise performance of our technique with other techniques proposed earlier for noise immunity enhancement in domino gates in terms of trade-off parameters. Lack of process uniformity in silicon manufacturing, variation in supply voltage and temperature cause variability in circuit delay performance and becomes major concerns of deep sub-nanometer regime [13]. To demonstrate effectiveness of our technique in deep sub-nanoscale regime, influence of PVT (process-voltage-temperature) variations on our technique is also examined. Simulations were conducted for 8 i/p AND gate as a bench mark wide fan in digital circuit and the results are confirmed in *90 nm* technology.

Organization of the paper is as follows: In Section 2, we examine different circuit configurations with the approaches for noise immunity enhancement in order to corroborate that shortening the evaluation period can be coupled with raising threshold voltage for enhancing noise tolerance with controlled overheads. We present implementation and operation of the proposed technique in Section 3. Section 4 describes the environment adopted for our simulation based experiments. Simulation results are analyzed in Section 5, in order to compare the performance of the proposed technique with other techniques considered in this paper. We also investigate here influence of PVT variations on delay performance of our circuit configuration.

Related work

Noise in dynamic (domino) gates

Major sources of noise in deep-submicron technology are crosstalk (input) noise, leakage noise, supply noise and charge-sharing noise. However, noise sources in dynamic circuits are broadly classified under two major categories: Gate internal noise and external noise (input noise) [3]. Gate internal noise occurs primarily due to (i) leakage noise referring to the charge loss caused by flow of leakage current from the off-state PDN transistors in evaluation phase [7, 14] and (ii) charge sharing caused by charge redistribution between the dynamic node and the internal nodes of PDN that may produce potential false switching at the output node [18]. Leakage noise is important for wide fan-in OR gate circuit configurations, where the evaluation transistors are connected in parallel [15, 17, 18] and simultaneously leak charge from the internal node. Charge sharing is a greater concern for wide fan-in AND configuration, where the evaluation transistors are connected in series. Various charge keeper based techniques have been published in literature [20-24] to sustain gate internal noise.

External noise is the noise presented at the inputs of domino gates. It is caused by coupling effect i.e. crosstalk among adjacent signal wires occurring because of the insistent interconnect scaling in lateral dimension with relatively unchanged vertical dimension [19]. Redistribution of charges from the internal node because of the external noises degrades the voltage level at the dynamic node and produces error. In all, these noises lead to severe impact on usefulness of domino gates.

Noise tolerant domino techniques

External noise is a prominent source of failures in deep submicron technologies [3]. Noise tolerances characteristics shown in Fig. 1 [10] indicate that magnitude and pulse width of external noise determine probability of erroneous results. Accordingly, raising the threshold voltage V_T of the evaluation transistor [8-10] and controlling the evaluation period using delayed clock [11, 12] are found effective schemes to enhance noise tolerance of domino gates.

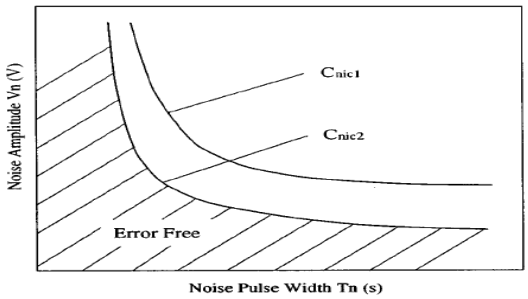


Fig. 1: Noise immunity curve

Fig. 2 (a) depicts AND2 circuit using Bobba's technique [8]. Combination of additional nMOS and pMOS transistors at source nodes N1 and N2 creates a static inverter, which forms a voltage divider. As a result, V_T of the evaluation transistors equals V_T of the static inverter that is close to $V_{DD}/2$. This higher switching threshold reduces effect of input (external) noise as the noise pulse requires a larger magnitude in evaluation phase. Power consumption of this technique is very high because of (i) the use of two additional transistors per evaluation transistor and (ii) precharging of the internal nodes from G_{ND} to V_{DD} if they are discharged. Two series nMOS transistors per evaluation transistor in discharging path and the increased capacitance at gate inputs due to the additional pMOS transistors lead to delay penalty.

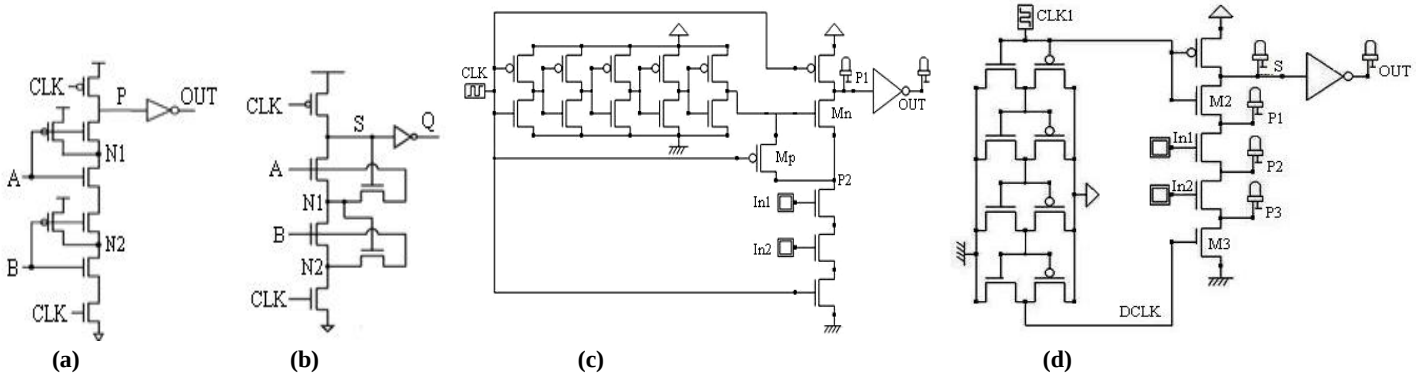


Fig. 2: (a) Bobba's technique [8] **(b)** Twin-transistor technique [10] **(c)** Mendoza technique [11] **(d)** Mazumdar's technique [12].

Twin-transistor technique [10] shown in Fig. 2 (b) also improves noise immunity by pre-charging the internal node. Each evaluation transistor requires single additional pre-charge (pull up) nMOS transistor to increase voltage level (V_{SBn}) of source terminals N1 and N2. Higher V_{SBn} has two effects: (i) Gate turn ON voltage increases, as it must be greater than sum of the source voltage and the threshold voltage (V_T). (ii) V_T of each evaluation transistor increases due to body bias effect as per Eq. (1) [25].

$$V_T = V_{TO} + \gamma(\sqrt{|V_{SB} + 2\phi_F|} - \sqrt{|2\phi_F|}) \qquad (1)$$

Unlike Bobba's technique, in this technique the drain nodes of pre-charge transistors are pulled up to the inputs instead of power supply to avoid unnecessary injection of current and lower the gate power consumption. This pull up of the transistors increases load capacitance of the gate input drivers and slows down switching of gates. For wide fan-in, such technique is not suitable as it requires one extra transistor per evaluation transistor causing area and power penalty. Further, input nodes are short circuited in this technique for implementation of certain logic functions [3]. e.g. (A+B).C.

Mendoza technique [11] combines the approach of shortening the evaluation period along with pre-charging the internal nodes (to reduce the leakage noise). As shown in Fig. 2 (c), transistor M_p pre-charges the internal node P2 to reduce the impact of leakage noise. Clock is delayed and inverted with the help of inverter delayed chain logic (IDL). IDL turns off M_n in the middle of the evaluation phase, which virtually isolates the node P1 from the inputs (Phase IV in Fig.3).

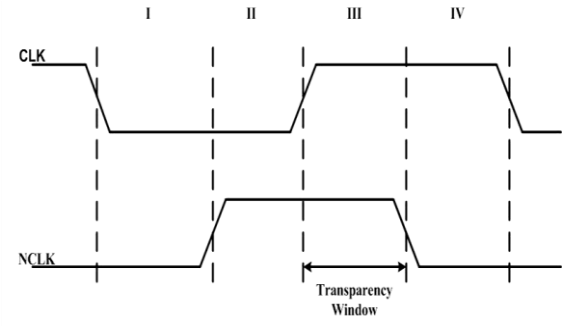


Fig. 3: CLK based circuit operation

Dynamic node discharging time of the circuit is dependent on turn on time period of the transistor M_n. This time period referred to as *transparency window* increases for wide fan-in circuit configurations. The extended window leads to penalty in delay and power due to increase in IDL inverters. Increase in inverters widens the *transparency* window further. Enlarged *transparency window* makes the circuit more susceptible to noise pulse duration. While the technique is pre-charging the internal node to reduce leakage noise, it does not raise the switching threshold of the evaluation transistors to enhance immunity against the magnitude of external noise signal appearing at the gate inputs.

Mazumdar's technique [12] attempts to enhance noise tolerance by shortening the evaluation period only. As shown in Fig. 2 (d), clock is simply delayed with the help of IDL to shorten the evaluation period. As a result, number of IDL inverters is reduced in comparison with Mendoza technique [11]. The technique retains M2 of Mendoza technique in between the pre-charge and the evaluation transistors to limit leakage noise.

IDL inverters added to support wide fan-in circuits will delay DCLK further and decrease the period of *transparency window* as shown in Fig. 4. Note that, reduction in *transparency window* makes the circuit using this technique more immune to noise in contrast to Mendoza technique which extends the period in case of wide fan-in configurations. Period of Phase IV is also longer, where low CLK turns off M2 and isolates the dynamic node from input transistors.

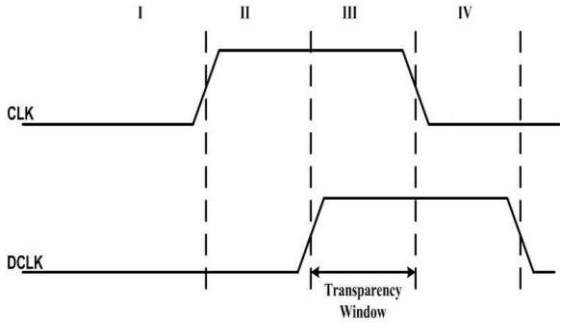


Fig. 4: CLK based circuit operation

Table 1 summarizes the implementation cost of various techniques for noise immunity enhancement in domino gates. Requirement of large number of transistors in Bobba's and Twin Transistor techniques clearly indicates their inappropriateness for wide fan-in circuits as compared to Mendoza and Mazumadar's technique.

Table 1: Transistor counts

	Techniques			
	Bobba's Tech.	Twin Transistor Tech.	Mendoza Tech.	Mazumdar Tech.
AND2	10	9	18	15
AND8	28	20	24	21
AND16	52	36	30	27

Mazumadar's technique appears to be more cost effective than other techniques in case of wide fan-in circuits i.e. AND 16. In order to identify scope of further enhancement of noise immunity of wide fan-in configurations, we examine operation of the circuit using Mazumdar's technique below. PDN of the circuit configuration shown in Fig. 2(d) is turned on at the beginning of the evaluation phase (Phase II of Fig. 4) either by input signals or noise pulses. Transistor M2 is also turned on by high CLK and M3 is off due to delayed low DCLK at the same time. This increases voltage levels at the internal nodes (P1, P2, P3) of PDN because of charge sharing between the capacitance of the dynamic node and the parasitic capacitances of the internal nodes as shown in Table 2. Rise in voltage levels at the internal nodes increases source voltages (V_{SBn}) and V_T of each evaluation transistor.

Table 2: Internal node voltages (VDD= 1.2 V)

Internal nodes	Voltage levels (V)
P1	0.543 V
P2	0.540 V
P3	0.538 V

Note that higher V_{SBn} is obtained without pre-charging the internal node. V_{SBn} and subsequently V_T can be increased further if the internal node is pre-charged during the evaluation phase before the *transparency* window computes.

The proposed modifications

In this section, we propose a modification in Mazumadar's technique [12] to pre-charge the internal node with the help of an additional transistor in order to restrict the impact of noise signal occurring during the evaluation phase.

Operation of our technique

Fig. 5 illustrates the circuit configuration using Mazumdar's technique [12] altered by the additional transistor M_N. Transistor M2 turned ON by high CLK and M3 turned OFF by low DCLK prevent the discharging of dynamic node capacitance (Refer Phase II of Fig. 4). In the beginning of evaluation phase, the additional transistor M_N pre-charges the internal node and increases V_T for protection against noise signal. PDN of the proposed circuit configuration in presence of the modifications is given in Fig. 6. PDN consists of 2 input AND gate with three internal nodes P1, P2, P3. Note that our technique is consistent with CLK based circuit operation adopted by [12].

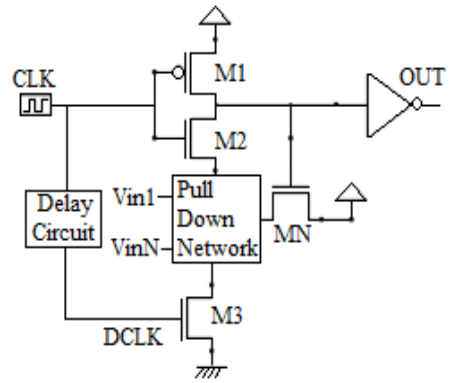


Fig. 5: Schematic of the proposed modification

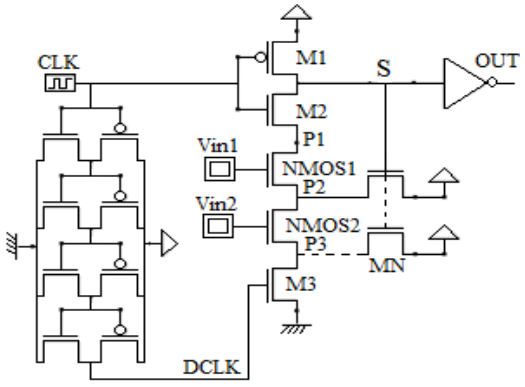


Fig. 6: Node selection for the pre-charge transistor

The additional transistor M_N can be affixed to the internal node (i.e. P2 or P3) to produce a higher V_T of the evaluation transistors. If M_N is connected to the node P3, M_N and M3 are simultaneously turned ON with high CLK and DCLK (*transparency window*). In this situation, short circuit current flows from V_{DD} to G_{ND} irrespective of input conditions, leading to higher power dissipation. Moreover, the parasitic capacitance formed at P3 is continuously charged by M_N and discharged by M3. This reflected in measurement of voltage levels at the nodes P2 and P3 found as 0.877 V and 0.730 V respectively, while keeping the additional transistor at these nodes alternately.

If M_N is connected to the first source node (P2) of PDN, the short circuit current is blocked by the lower evaluation transistor (NMOS2), according to the input condition (1, 0). The same benefit is available if one of the series evaluation transistors of wide fan-in configurations is turned-off depending upon the noise condition. Thus, P2 offers benefit in terms of power dissipation besides the higher voltage levels (V_{SBn}). Therefore, the first source node of PDN in general is the appropriate position as it increases V_{SBn} without much expense in power. Selection of the node P2 is substantiated with the help of simulation results in Appendix I.

In summary, the additional transistor M_N at node P2 in the modified circuit arrangement enhances the switching threshold of evaluation transistors before the evaluation period is shortened with Mazumdar's technique. Our proposed technique has two fold benefits: (1) It retains the shortened evaluation period to reduce susceptibility to the pulse width of noise signal. (2) It offers higher switching threshold of the evaluation transistor to improve protection against the magnitude of noise signal. This in turn, enhances overall noise immunity of wide fan-in domino gates. In the next section, we discuss simulation environment and methodology used for our experiments.

Simulation environment

Different noise tolerance enhancement techniques discussed earlier in this paper are implemented using small and wide fan-in (AND2 and AND8) benchmark circuits. The circuits are implemented and simulated by using SPICE tool [26]. Microwind 3.1 tool is used to evaluate post silicon area consumed by various techniques [26]. Functionalities of the circuits are verified and subsequently various design metrics like noise immunity, power, delay, and area are evaluated. Pulses of external noise are applied to all inputs of PDN in the evaluation phase. Since impact of the noise signal is decided by its amplitude and pulse duration (critical in wide fan-in circuits due to longer evaluation period), we have used ANTE (Average Noise Threshold Energy) [27, 28] for noise immunity measurement as shown in Eq. (2) where, V_{noise} and T_{noise} represent amplitude and pulse duration of the noise signal respectively. Since, ANTE can corroborate noise immunity without including energy and delay penalty, trade-off metrics ANTE/Delay and ANTE/Power [12] are also computed to demonstrate overall noise performance.

$$ANTE = E\,(V^2_{noise} T_{noise}) \qquad (2)$$

Table 3: Simulation parameters

Parameter	Specification
Technology	90 nm
V_{DD}, V_{TP}, V_{TN}	1.2V, 0.32 V, 0.28V
i/p voltage	1.2V
Temperature	27 ºC
Noise immunity	ANTE
Trade-off parameter	ANTE/delay & ANTE/Power
CLK	1 GH_Z
Noise Pulse Gate-oxide thickness Channel length	External (cross-talk) type 2nm 90nm
i/p pattern	same as per CLK pattern

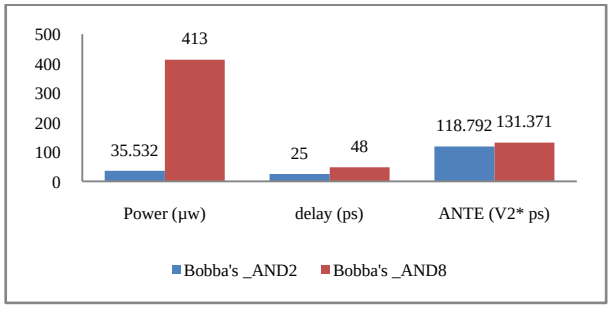
Lack of process uniformity in silicon manufacturing, variation in supply voltage and temperature cause variability in circuit performance in deep sub-nanoscale bulk-Si MOSFET based configurations [13, 29]. PVT variations refer to the deviations of the circuit parameters from their nominal value [30]. PVT (Process-Voltage-Temperature) variations for the proposed technique are modeled using a ±15% Gaussian distribution for parameters like gate oxide thickness, channel length, threshold voltage, supply voltage and temperature. Impact of these variations is analyzed with the help of Monte Carlo simulation, which is useful for simulating the effects of process variations on circuit performance. For each sample (sample size of 30) of the analysis, random values are

assigned to the above stated parameters and a complete simulation is executed.

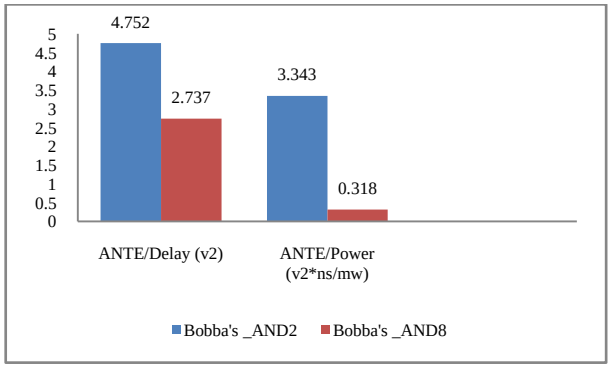
Performance comparison

In this section, we present simulation results of the noise performance of various techniques taken into consideration. Our focus is on the impact of different solutions proposed for noise immunity enhancement on overheads in design metrics of wide fan-in circuit configuration (AND8). Additionally, we also demonstrate effectiveness of our technique in deep sub-nanoscale regime by measuring the influence of PVT (process-voltage-temperature) variations in circuit delay performance of our technique.

In view of the fact that Bobba's technique has demonstrated superior noise performance for small fan-in [17], we first examine its relative performance for AND8 (wide fan-in circuit configuration) with reference to (AND2). Fig. 7 (a) shows a marginal benefit in ANTE against huge cost in power consumption of wide fan-in circuit (AND8) due to duplicated nMOS transistors for each input of Bobba's circuit configuration. The configuration also suffers in delay due to extra pMOS transistors causing higher capacitance at the gate input of PDN. Meager noise performance is achieved with the measured area of 106.1 μm^2 and 1952.1 μm^2 for AND2 and AND8 respectively. Poor trade-off factors of Bobba's technique for AND8 in Fig. 7 (b) also confirm unsuitability for the wide fan-in circuits. In view of the inconsistent performance of Bobba's technique, we compare the noise performance of our technique with Mendoza and the baseline Mazumdar's technique with reference to effect on design metrics.



(a) Design metric



(b) Trade-off factors

Fig. 7: Performance of Bobba's circuits

Performance comparison of wide fan-in circuit configurations:

Since V_{SBn} plays a very important role in determining the noise immunity of gates, we first compare our observations for different techniques in this regard. As observed in Table 4, Mazumdar's technique has higher ANTE in comparison with Mendoza technique. Note that higher ANTE is achived because of reduction in the *transparency window* as discussed in Section 2 inspite of lower V_{SBn}. The modification proposed in Mazumdar's technique additionally pre-charges the internal node and produces a considerably higher V_{SBn} at the first source node, which is highest among V_{SBn} of all techniques. This along with *transparency* window reduced by Mazumdar's technique translates in to a significantly higher ANTE as compared to other two techniques. V_{SBn} at other source nodes were also observed to be higher in our technique. As a result, V_T of all evaluation transistors increase relatively and the overall noise immunity of the circuit also improves in presence of our modifications.

Table 4: Internal node voltages of various techniques

Techniques	ANTE (V^2 * ps)	V_{SBn}	
		First source node	Last source node
Mendoza	28.761	0.399	0.086
Mazumdar	30.456	0.389	0.035
Proposed	157.722	0.869	0.096

In order to confirm suitability of the proposed technique in wide fan in circuits, we examine impact on design metrics like power, delay and area. Fig. 8 (a) shows marginal rise in power and area overheads in our technique in comparison with Mazumdar's technique due to the additional transistor. The proposed technique retains the benefit of occupying considerably less area as compared to that of Mendoza technique. Capacitance of the additional transistor adds to the capacitance of the dynamic node and increases delay of circuit using our technique. However, significant relative improvement of 291.31% in ANTE of our technique as compared to Mazumdar's compensates the increase in delay. Higher trade-off factors of the proposed technique demonstrated in Fig. 8 (b) confirm this in order to defend the rise in overheads for significant enhancement in noise immunity of wide fan-in circuit configuration.

Impact of PVT Variations:

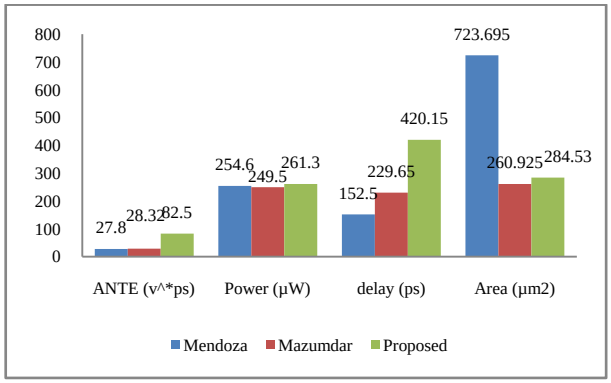
Inherent advantage of domino gate is superior delay performance compared to other counterparts [31]. Lithographic process variations are commonly observed in gate oxide thickness t_{ox} and channel length L_g. Variations in these parameters fluctuate eventually the transistor threshold voltage V_T, which has a critical role in circuit delay performance and leakage power dissipation [35]. In view of the fact that superior delay performance compared to other counterparts is inherent advantage of domino circuits, we investigate variation in circuit delay performance against variations in process parameters.

First, we demonstrate variations in the delay performance against ±15% variations in process parameters t_{ox} and L_g separately. Subsequently, we examine variations in delay performance against ±15% variations in V_T to represent the gross effect of variations in the process parameters.

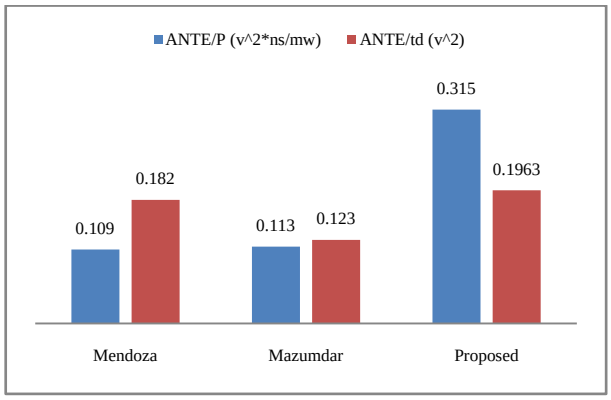
Variations in gate oxide thickness (t_{ox}) vary capacitive coupling (C_{ox}) between gate and substrate as well as V_T. With decrease in t_{ox}, C_{ox} increases and V_T also decreases, which in turn reduces the circuit delay. Fig. 9 shows that with ≠15% variations in t_{ox} from its nominal value of 2 nm, deviation delay tolerance window remains between +0.51% and -1.39% from its nominal value (420.15 ps).

In general, channel length (Lg) affects circuit delay of transistor. Circuit delay reduces as Lg reduces and vice-versa. As seen in Fig. 10, with ≠15% variations in L_g from its nominal value of 90 nm, deviation delay tolerance window lies between +0.51% and -4.01% from its nominal

value. Note that, systemic variation of channel length is applied to all transistors in the proposed configuration.



(a) Design metrics



(b) Trade-off factors

Fig. 8: Performance comparison

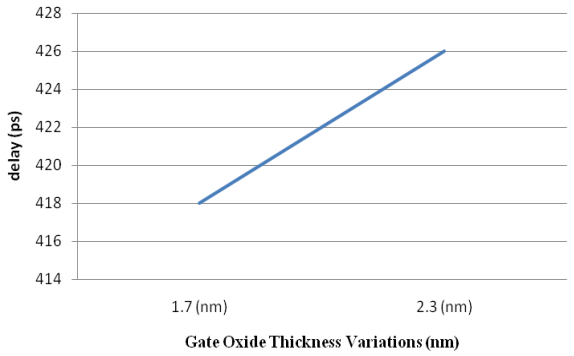


Fig. 9: Impact of variation in t_{ox}

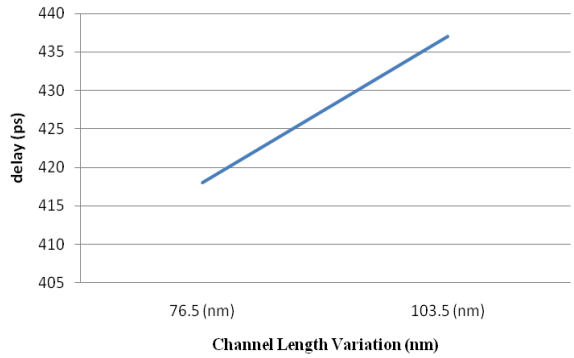


Fig. 10: Impact of variation in L_g

Circuit delay performance is majorly dependent on V_T of critical-path transistors. Delay performance of circuit configuration is improved if V_T of critical-path transistors reduces. As seen from Fig. 11, with ≠15% variations in V_T from its nominal value, deviation delay tolerance window lies between +5.83% and -3.77% from its nominal value. It is assumed that all devices (both P and N-type) are affeted similarly by the sysmatic V_T variation of circuit configuration.

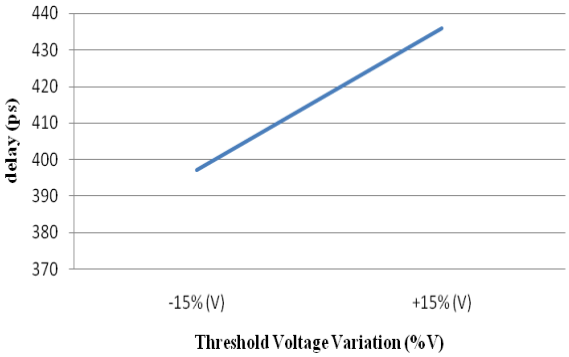


Fig. 11: Impact of variation in threshold voltage

Driving capability of circuit configuration reduces with lower supply voltages. Reduced driving capability in turn degrades the delay performance. It can be observed in Fig. 12 that with ≠15% variations in supply voltage from its nominal value of 1.2 V, deviation delay tolerance window lies between -0.82% and +0.27% from its nominal value.

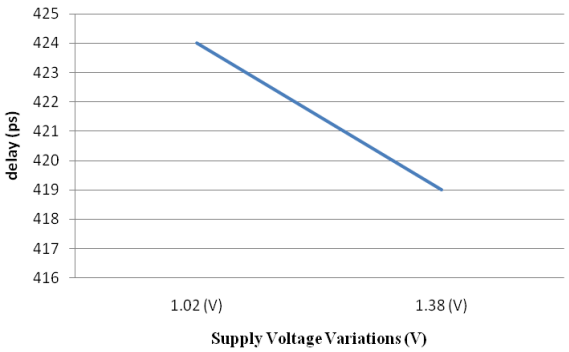


Fig. 12: Impact of variation in supply voltage

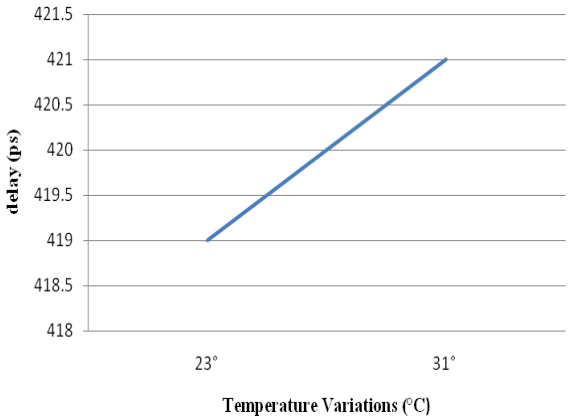


Fig. 13: Impact of variation in temperature

Carrier mobility and circuit delay performance degrade as the die temperature increases as shown in Fig. 13. With ≠15% variations in temperature from the nominal value of 27°C, deviation delay tolerance window remains between % +0.27% and -0.20% from its obtained value of 420.15 ps.

Circuit delay is more sensitive to variation in transistor V_T. Even the worst degradation in circuit delay lies between +5.83% to -4.01% and it is within acceptable limit. On average, there is no significant

degradation in circuit delay due to PVT variation within the limit of gaussian distribution considered here. Thus, the results of PVT analysis validate the suitability of our technique in deep sub-nanometer regime without causing significant degradation in the delay performance.

CONCLUSIONS

Our study of existing techniques reveals that Bobba's technique is inappropriate for wide fan-in configuration due to the requirement of large number of transistors. Our simulation results also confirm the negative impact of the transistor count on the overall performance of circuit configuration using bobba's technique which has shown better performance for small fan-in configurations.

This paper presents a modification in the noise enhancement technique proposed earlier by Mazumdar *et al*. [16]. Results of extensive simulations demonstrate a superior noise performance of the proposed technique for wide fan-in domino gates. Main contribution of our modification is to raise voltage at source of the evaluation transistor in order to increase the switching threshold voltage. The proposed modification exploits reduced *transparency* window of Mazumdar's technique for improving noise immunity of wide fan-in domino gates with a higher switching threshold.

Different existing noise enhancement techniques and our technique for domino gates are compared in 90nm technology. Our technique exhibits 291.31% improvement in ANTE over Mazumdar's technique. Relative improvement of 2.787 times in ANTE/Power and 1.595 times in ANTE/delay indicates that our scheme enhances noise immunity without significant cost in overheads in design metrics. Simulation results verify that PVT variations (≠15%) causes deviation in circuit delay performance of our technique lies between +5.83% to -4.01%.

Appendix I

As discussed in Section 3.1, node P2 or the first source node of PDN is suitable choice among all internal nodes for pre-charging while enhancing noise immunity in order to restrict the adverse effect on design metrics. Validation is confirmed by connecting M_N at all internal nodes (P1, P2 and P3) alternately and measuring ANTE *(*noise metric*)*, power and delay as shown in Fig. 9. ANTE observed by connecting the pre-charging transistor M_N to node P1 is much smaller than other two nodes. Since P1 is at the top of PDN, it cannot increase V_T of the evaluation transistor. Among P2 and P3, ANTE is observed to be higher by connecting M_N at P2 than at P3 since voltage obtained at P2 is reported higher in Section 3.1. If M_N is connected to node P3, M_N and M3 are simultaneously turned on in phase III. As a result, higher power dissipation occurs irrespective of input conditions. Therefore, node P2 or the first source node of PDN in general is the appropriate position for connecting pre-charging transistor because it increases V_{SBn} without much expense in power dissipation.

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